#3

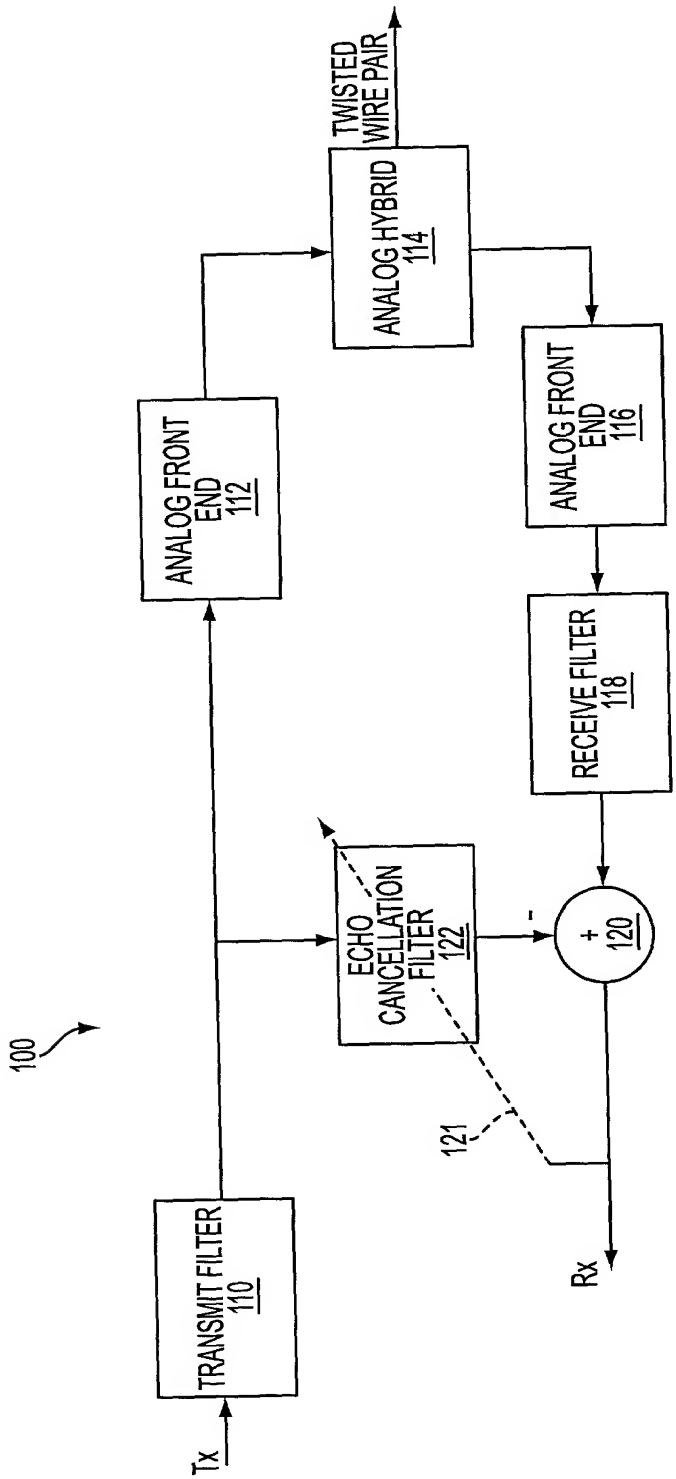
100
TRANSMIT FILTER 110
Tx
ANALOG FRONT END 112
ANALOG HYBRID 114
TWISTED WIRE PAIR
ANALOG FRONT END 116
RECEIVE FILTER 118
ECHO CANCELLATION FILTER 122
121
+ 120
-
Rx

FIG. 1A

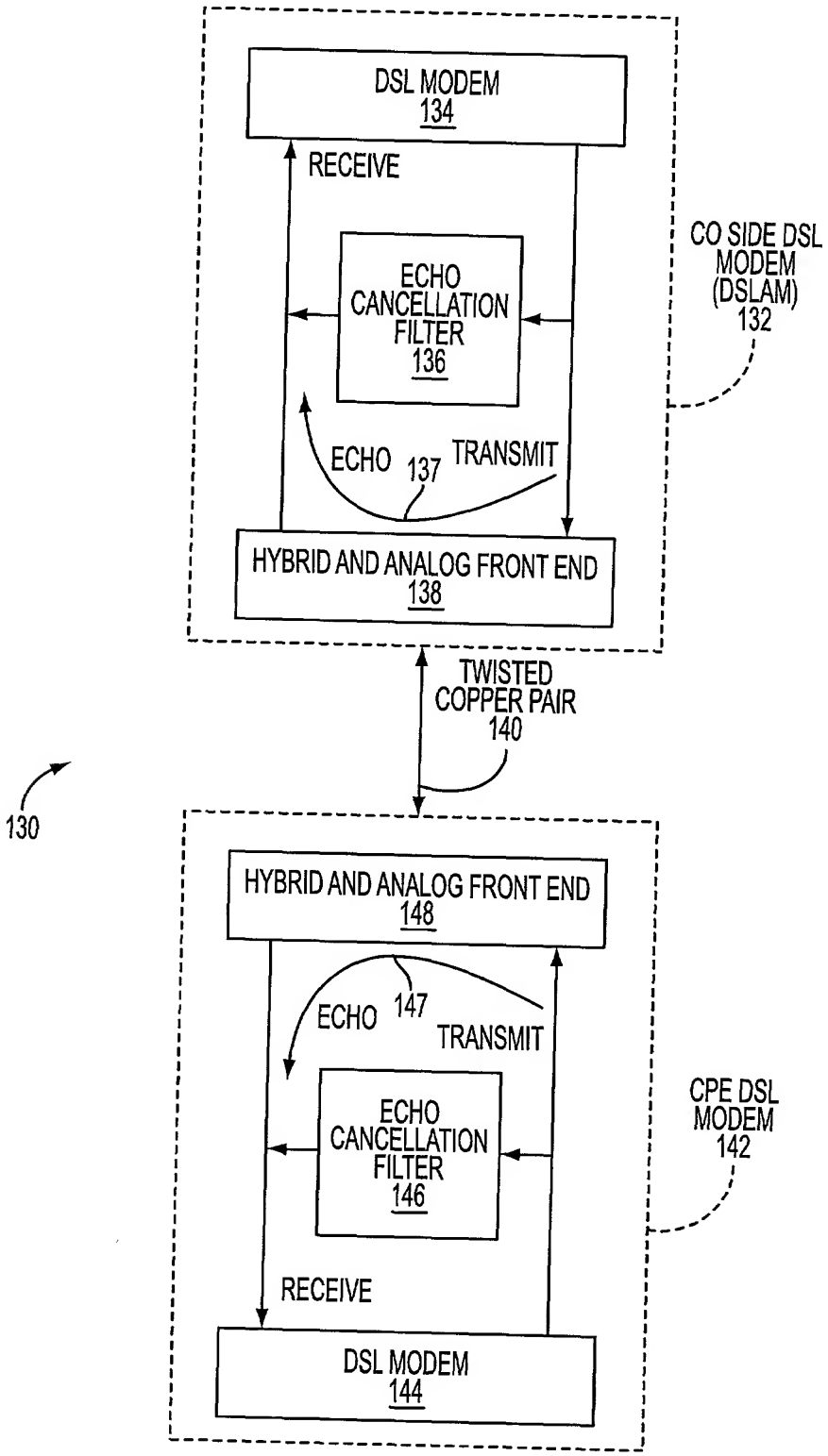
DSL MODEM
134
RECEIVE
ECHO
CANCELLATION
FILTER
136
CO SIDE DSL
MODEM
(DSLAM)
132
ECHO
137
TRANSMIT
HYBRID AND ANALOG FRONT END
138
TWISTED
COPPER PAIR
140
130
HYBRID AND ANALOG FRONT END
148
ECHO
147
TRANSMIT
ECHO
CANCELLATION
FILTER
146
CPE DSL
MODEM
142
RECEIVE
DSL MODEM
144

FIG. 1B

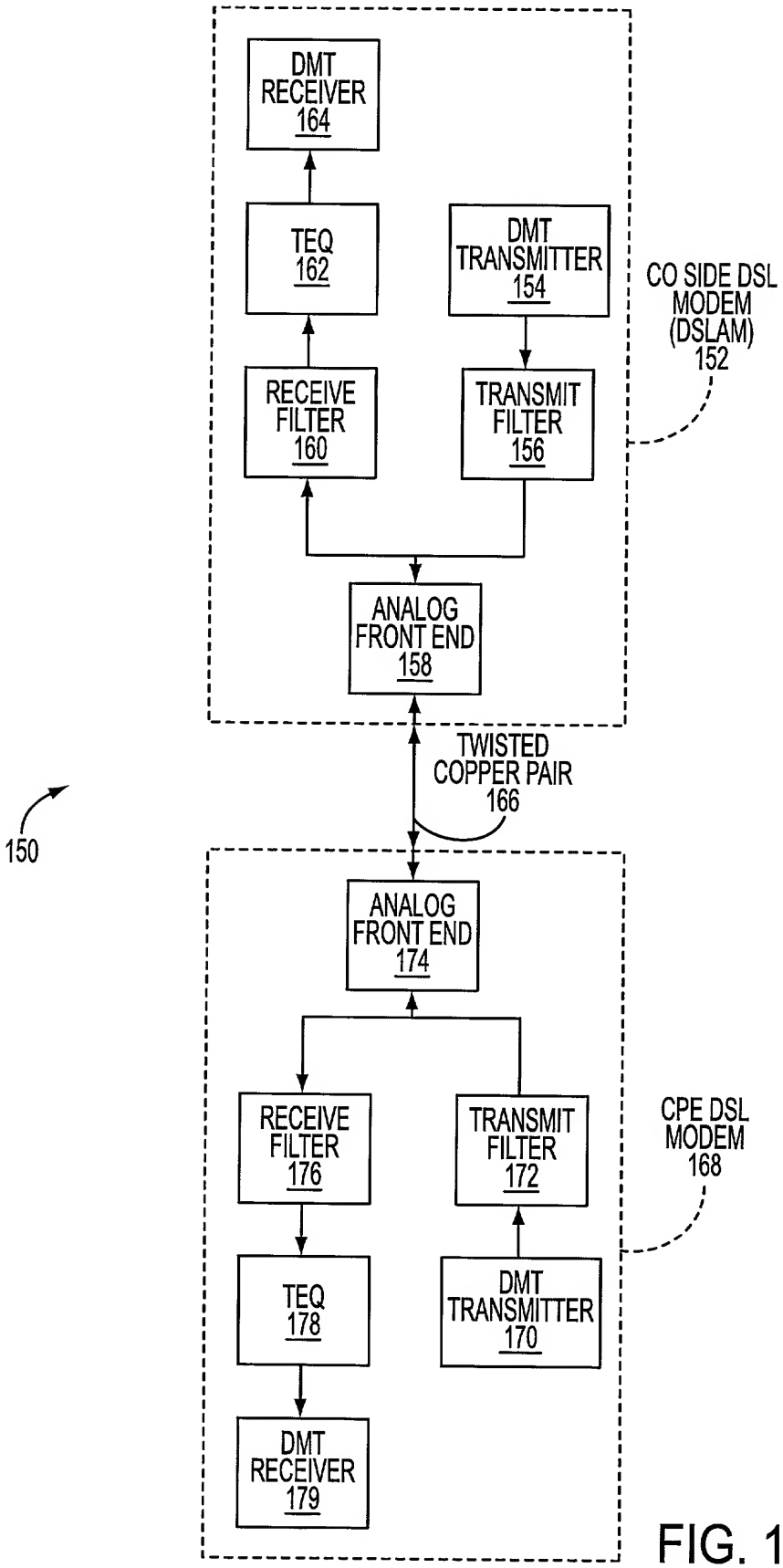
DMT RECEIVER 164
TEQ 162
DMT TRANSMITTER 154
CO SIDE DSL MODEM (DSLAM) 152
RECEIVE FILTER 160
TRANSMIT FILTER 156
ANALOG FRONT END 158
TWISTED COPPER PAIR 166
150
ANALOG FRONT END 174
RECEIVE FILTER 176
TRANSMIT FILTER 172
CPE DSL MODEM 168
TEQ 178
DMT TRANSMITTER 170
DMT RECEIVER 179

FIG. 1C

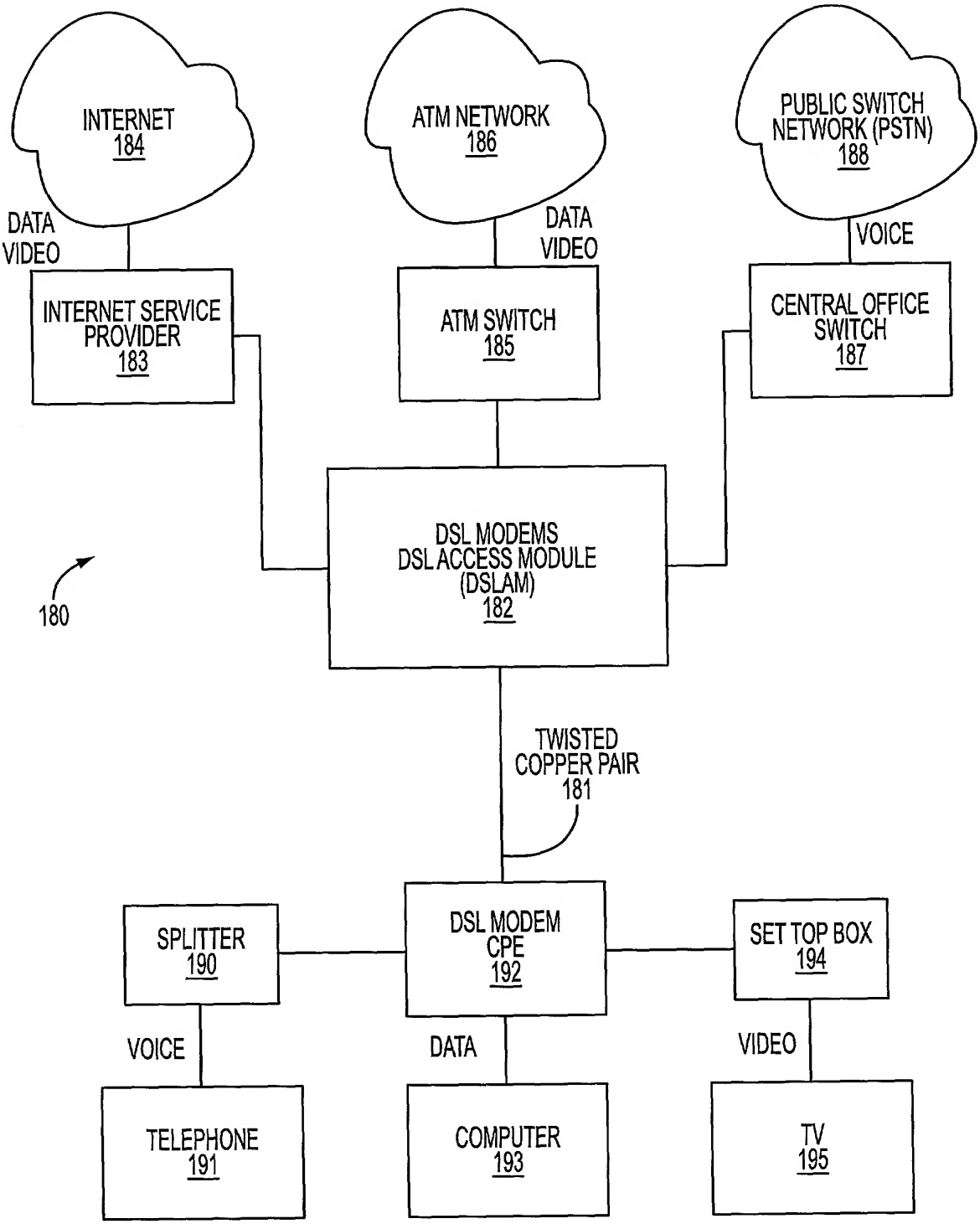
INTERNET
184
ATM NETWORK
186
PUBLIC SWITCH
NETWORK (PSTN)
188
DATA
VIDEO
DATA
VIDEO
VOICE
INTERNET SERVICE
PROVIDER
183
ATM SWITCH
185
CENTRAL OFFICE
SWITCH
187
DSL MODEMS
DSL ACCESS MODULE
(DSLAM)
182
180
TWISTED
COPPER PAIR
181
SPLITTER
190
DSL MODEM
CPE
192
SET TOP BOX
194
VOICE
DATA
VIDEO
TELEPHONE
191
COMPUTER
193
TV
195

FIG. 1D

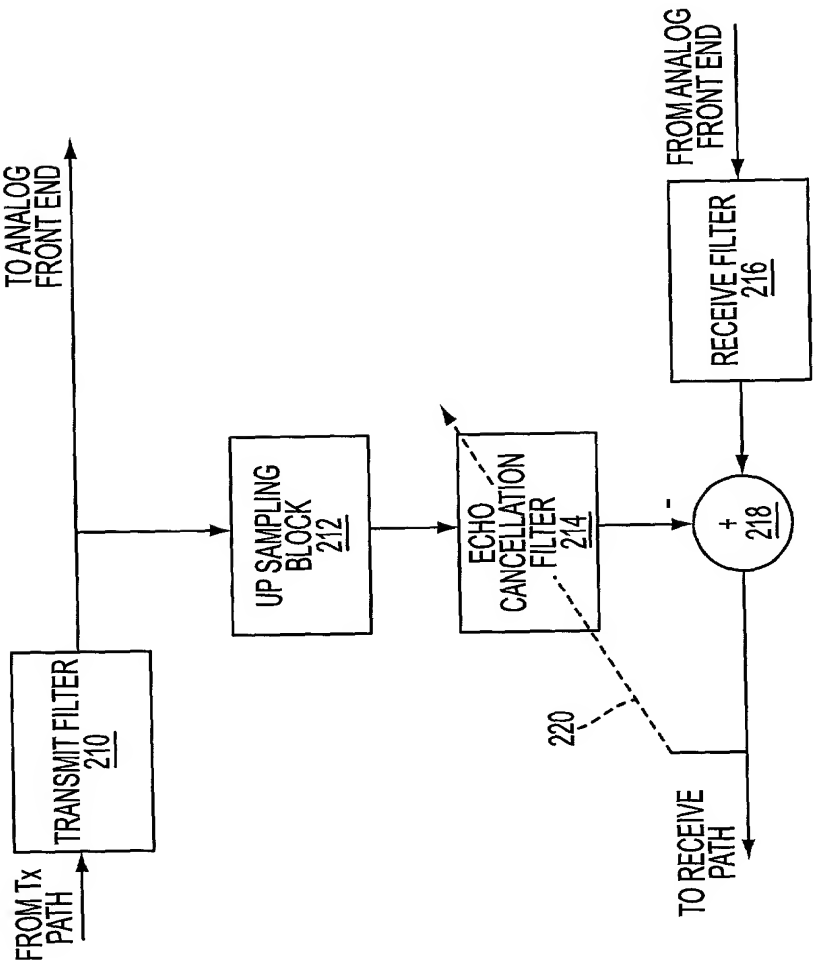
FROM Tx PATH
TRANSMIT FILTER 210
TO ANALOG FRONT END
UP SAMPLING BLOCK 212
ECHO CANCELLATION FILTER 214
220
FROM ANALOG FRONT END
RECEIVE FILTER 216
+
-
218
TO RECEIVE PATH

FIG. 2

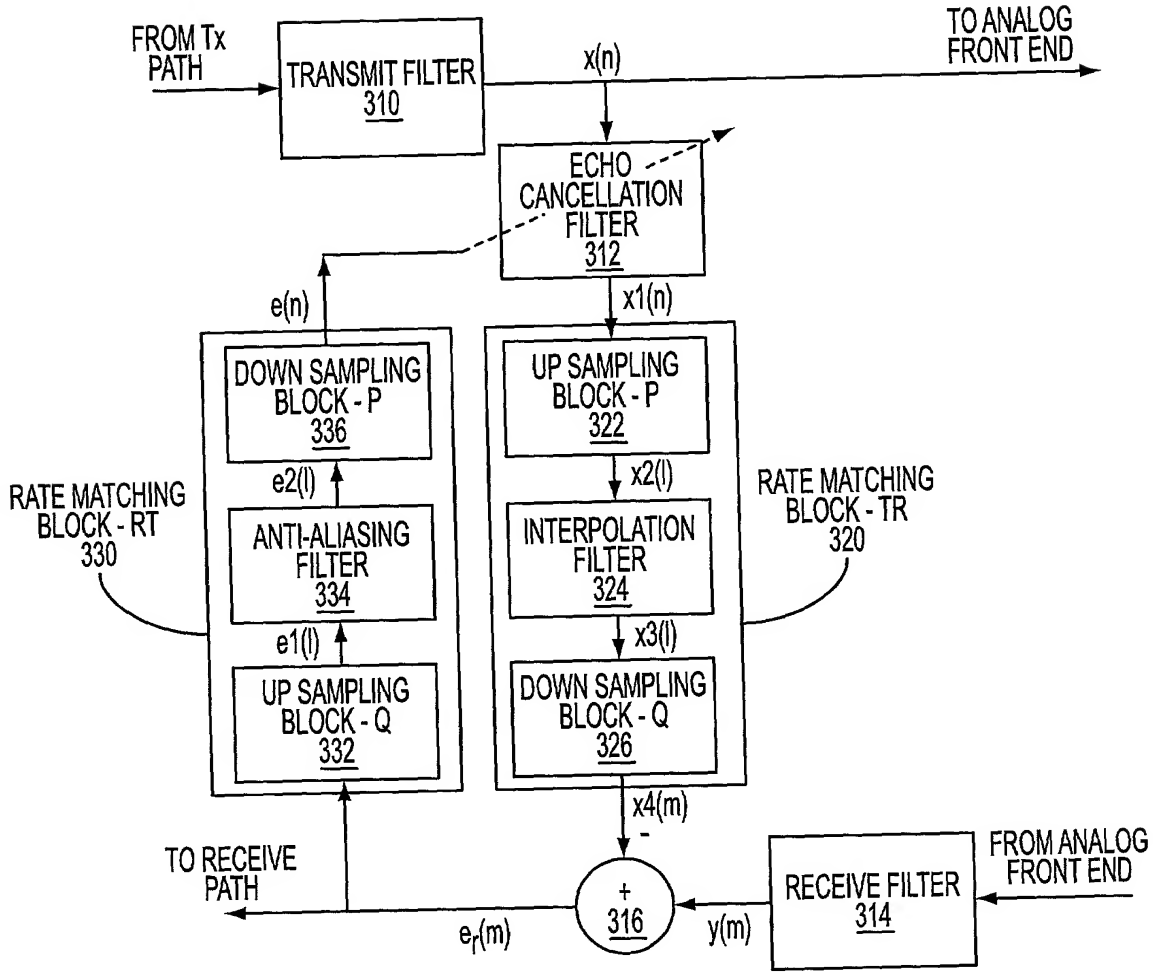

FIG. 3

Docket #56162.000357

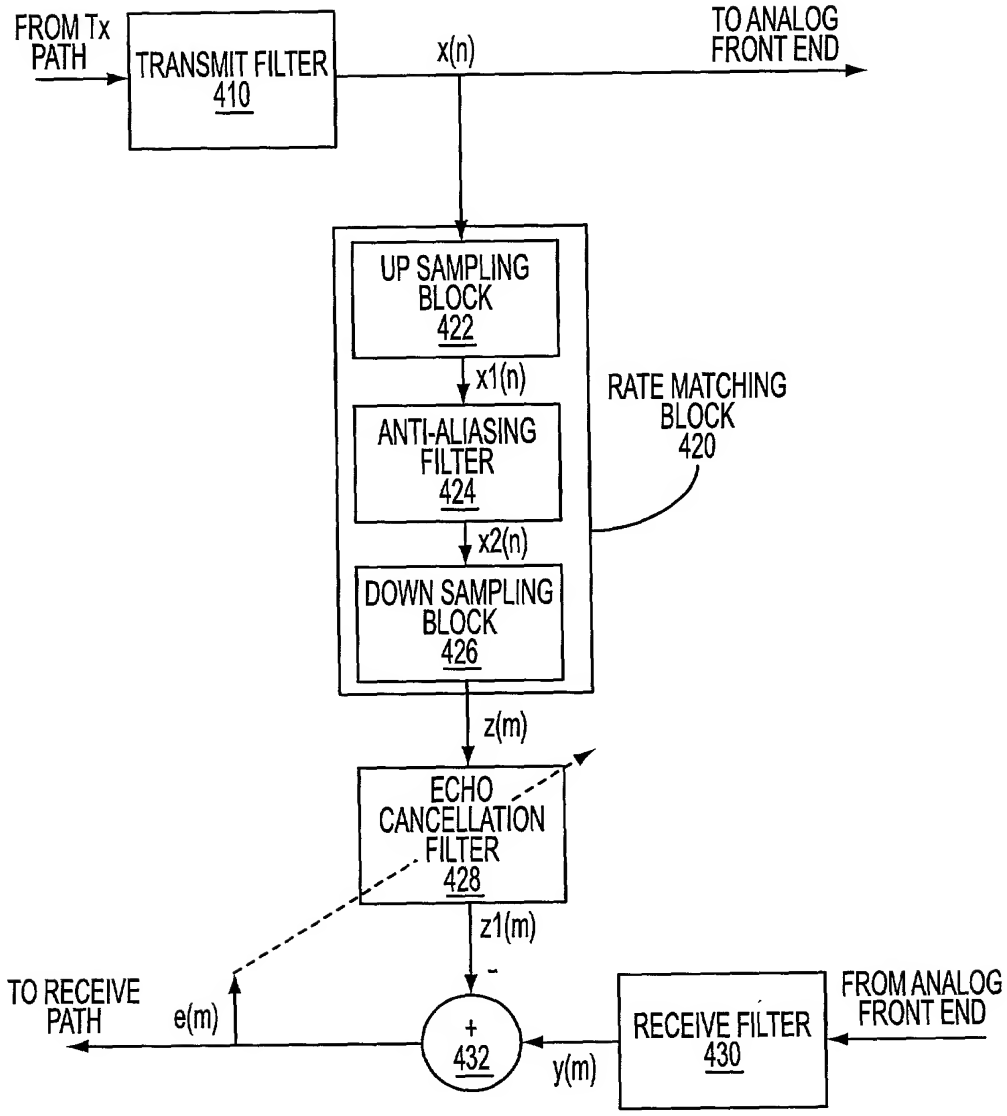
FROM Tx PATH
TRANSMIT FILTER 410
x(n)
TO ANALOG FRONT END
UP SAMPLING BLOCK 422
x1(n)
ANTI-ALIASING FILTER 424
x2(n)
DOWN SAMPLING BLOCK 426
RATE MATCHING BLOCK 420
z(m)
ECHO CANCELLATION FILTER 428
z1(m)
TO RECEIVE PATH
e(m)
+
432
-
y(m)
RECEIVE FILTER 430
FROM ANALOG FRONT END

FIG. 4

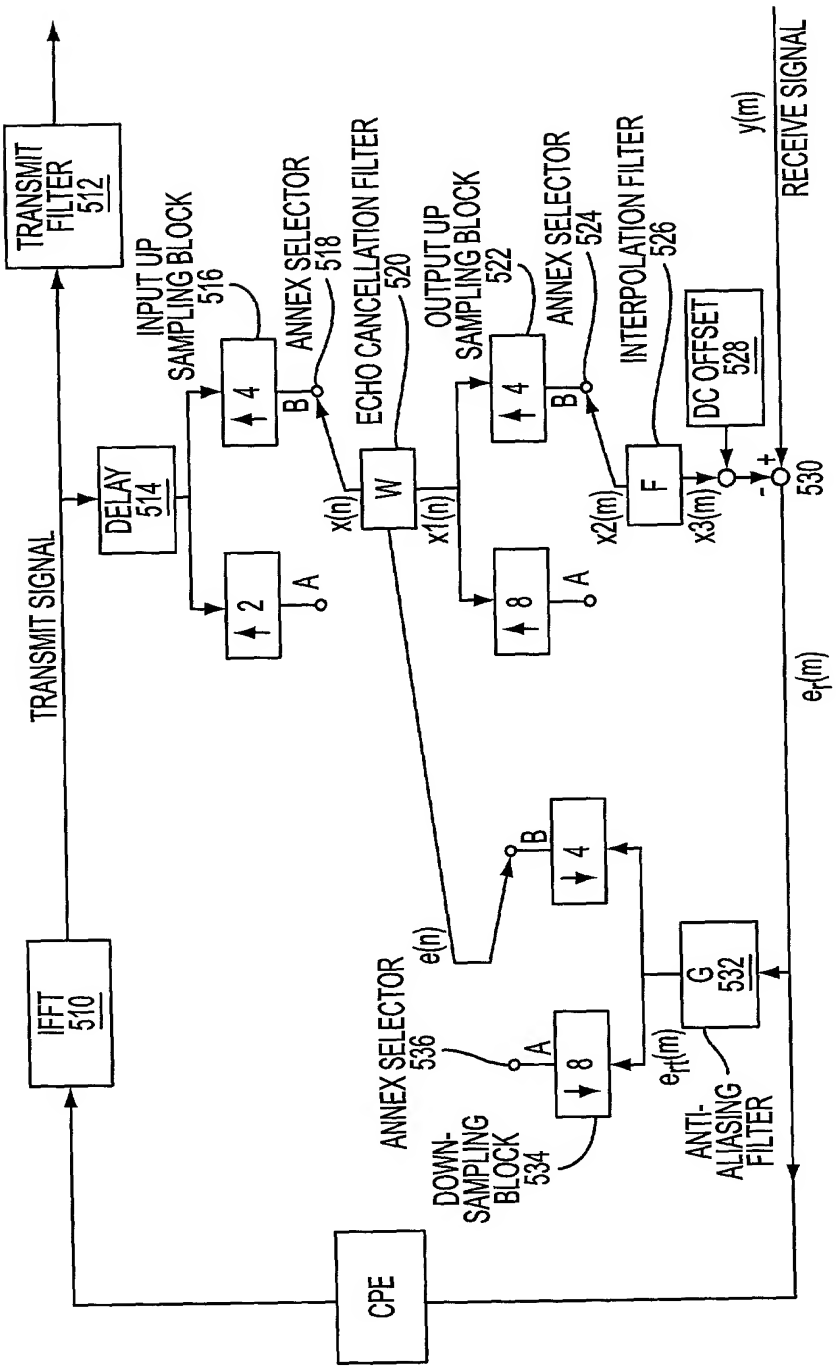
TRANSMIT FILTER 512
INPUT UP SAMPLING BLOCK 516
ANNEX SELECTOR 518
ECHO CANCELLATION FILTER 520
OUTPUT UP SAMPLING BLOCK 522
ANNEX SELECTOR 524
INTERPOLATION FILTER 526
DC OFFSET 528
RECEIVE SIGNAL
y(m)
TRANSMIT SIGNAL
DELAY 514
x(n)
W
x1(n)
x2(m)
F
x3(m)
530
IFFT 510
e(n)
ANNEX SELECTOR 536
DOWN-SAMPLING BLOCK 534
G 532
ANTI-ALIASING FILTER
CPE

FIG. 5

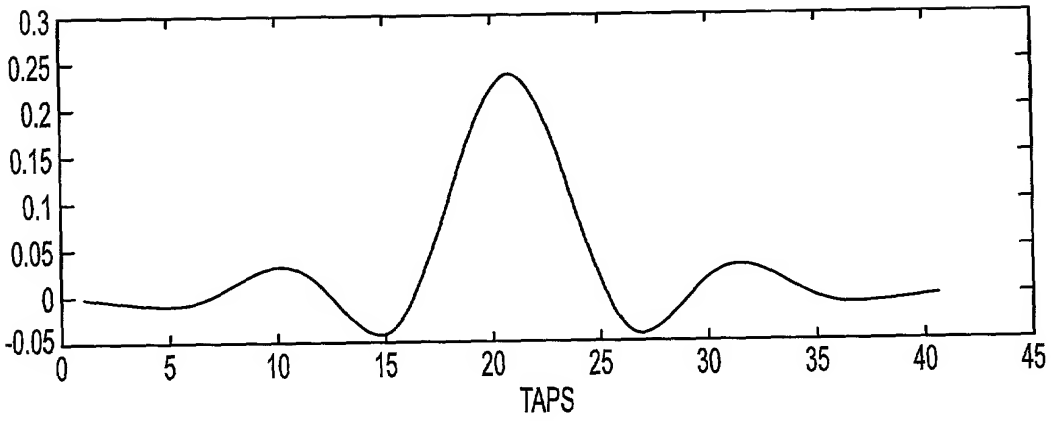
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
0
5
10
15
20
25
30
35
40
45
TAPS

FIG. 6

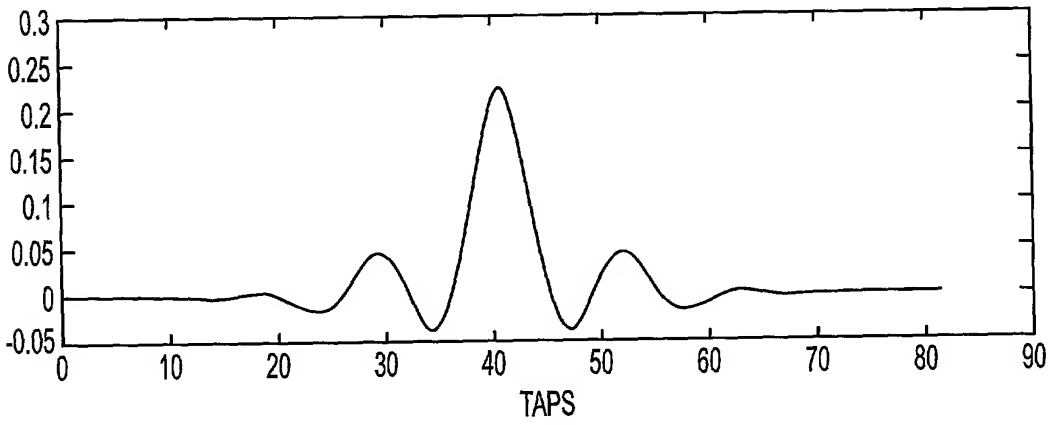
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
0
10
20
30
40
50
60
70
80
90
TAPS

FIG. 7

20020207040

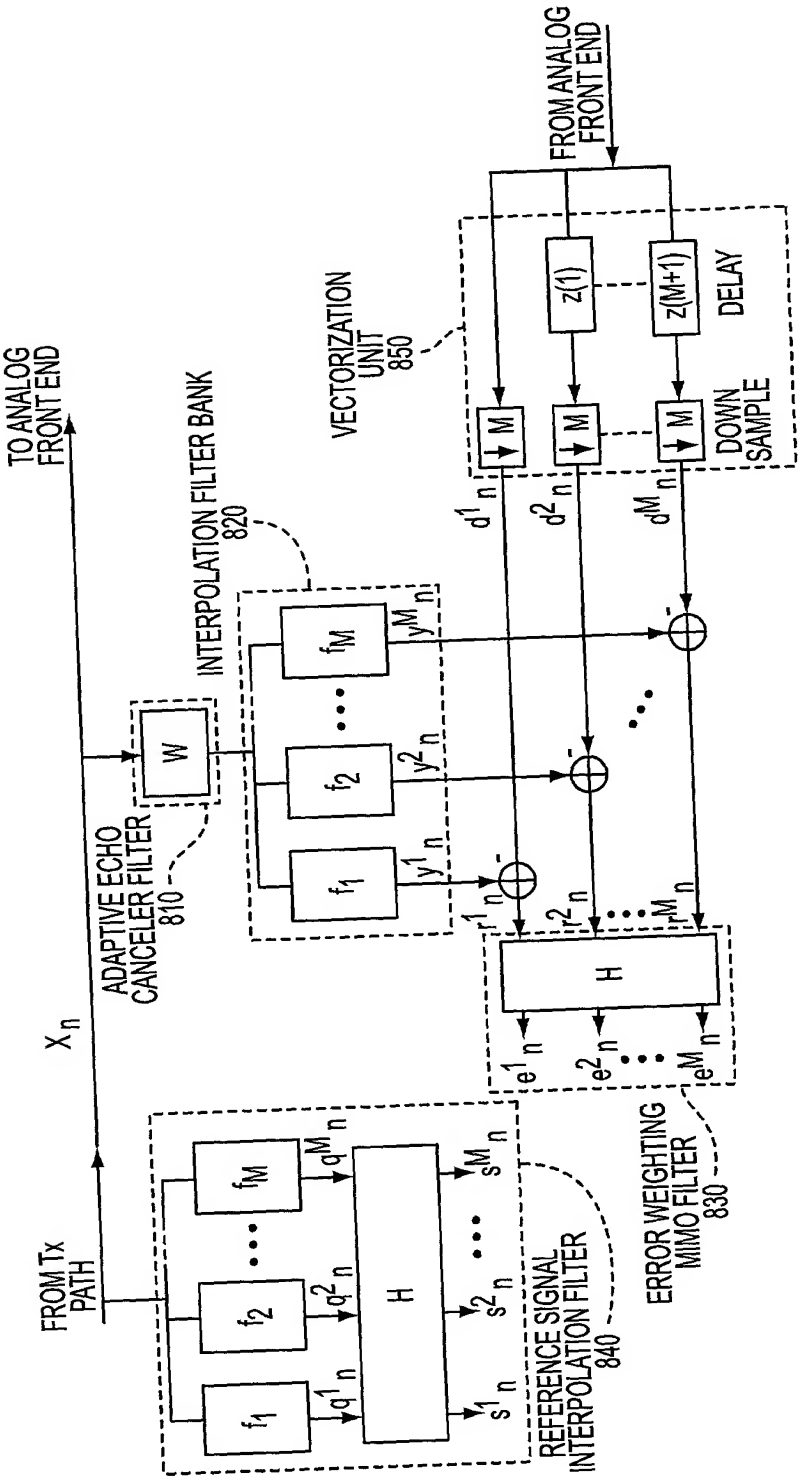

FIG. 8

10020172 - 020502

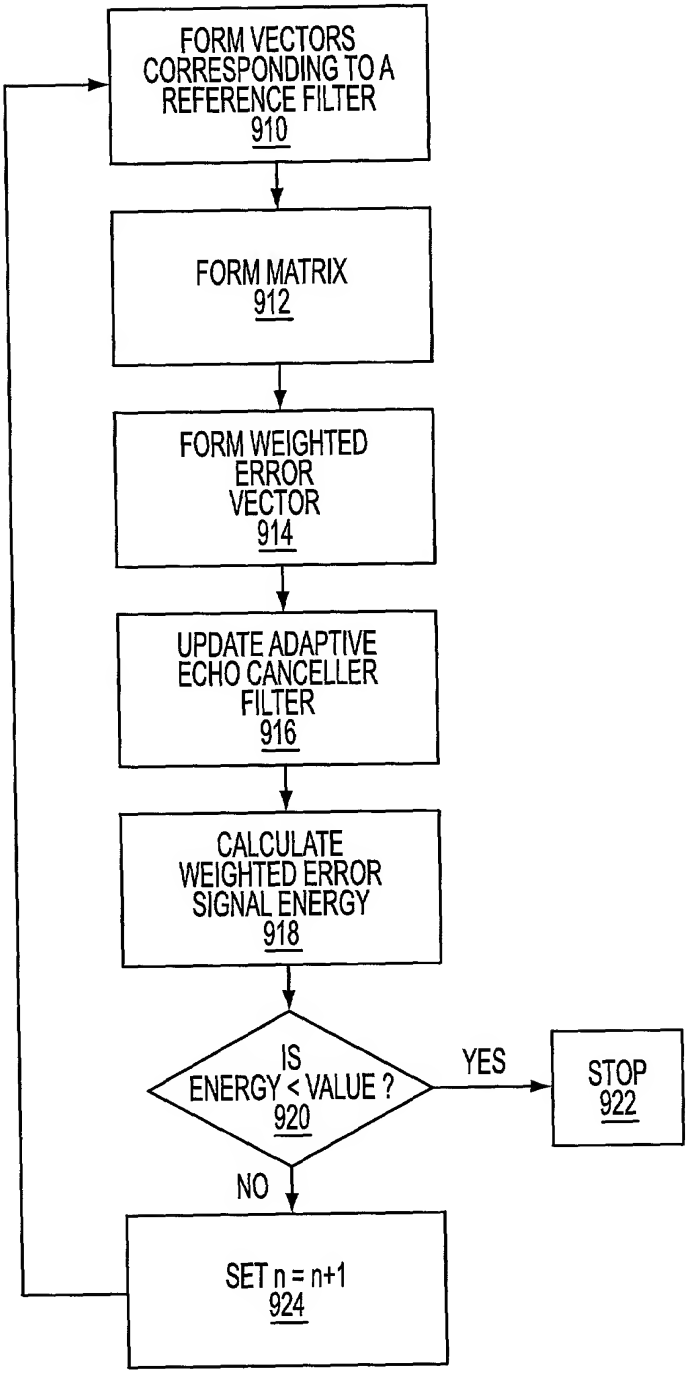

FIG. 9

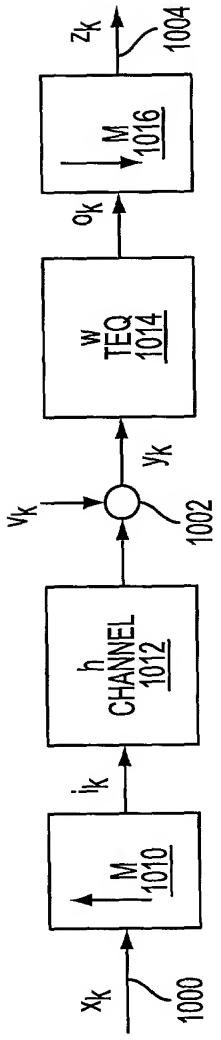

FIG. 10A

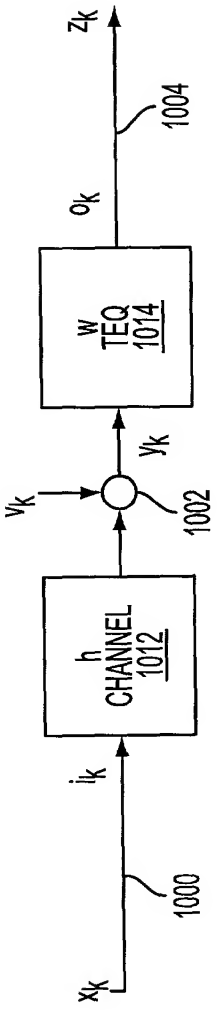

FIG. 10B

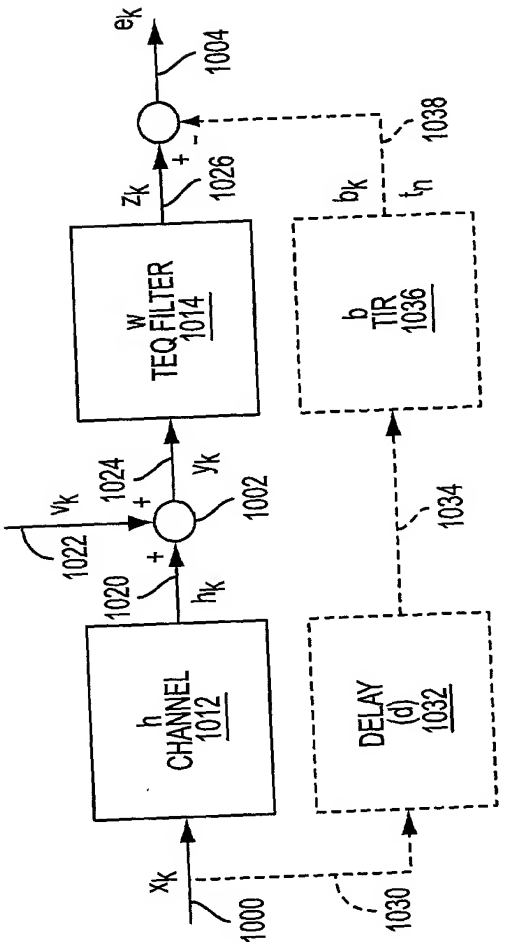
e_k
1004
1038
b_k
t_n
z_k
1026
w
TEQ FILTER
1014
b
TIR
1036
1024
y_k
v_k
1002
1022
1020
h_k
1034
h
CHANNEL
1012
DELAY
(d)
1032
x_k
1000
1030

FIG. 10C

EXPRESS MAIL NO. EV339950742

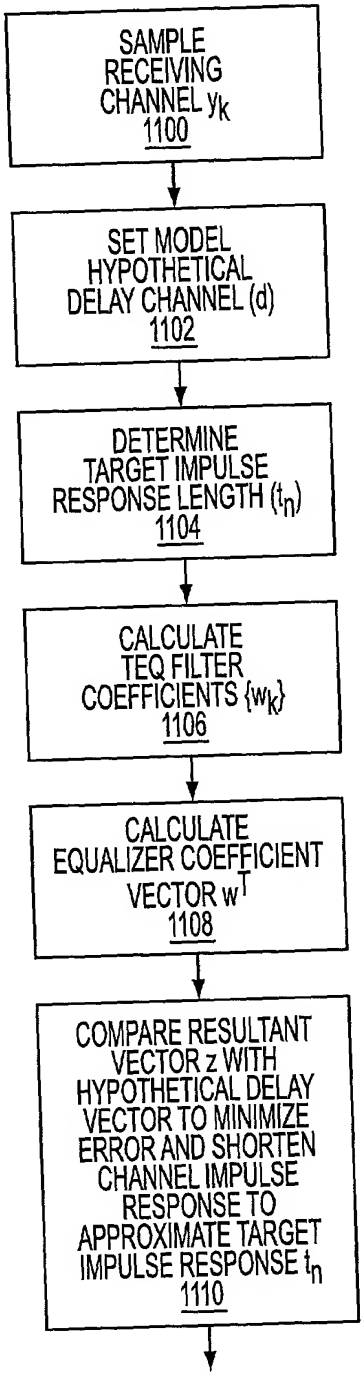

FIG. 11

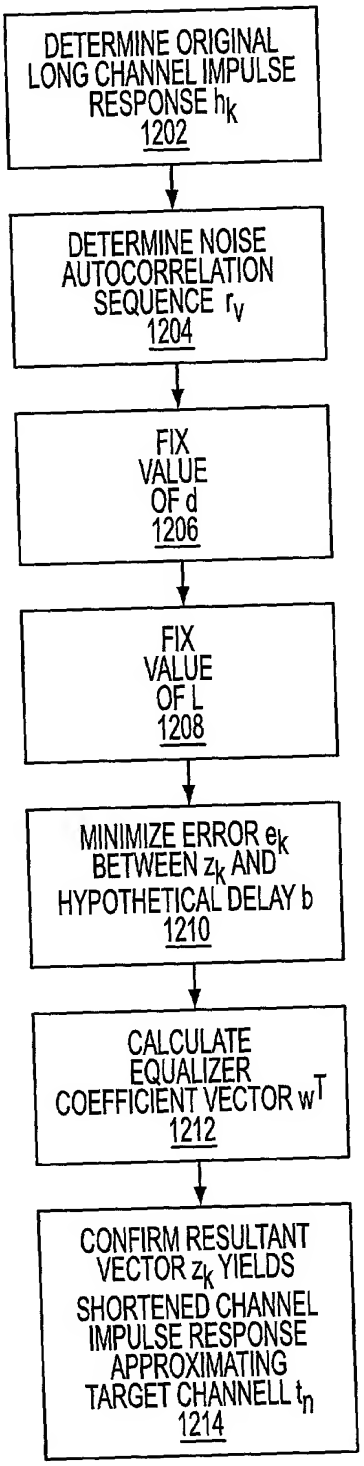

FIG. 12

EXPRESS MAIL NO. EV339050247US

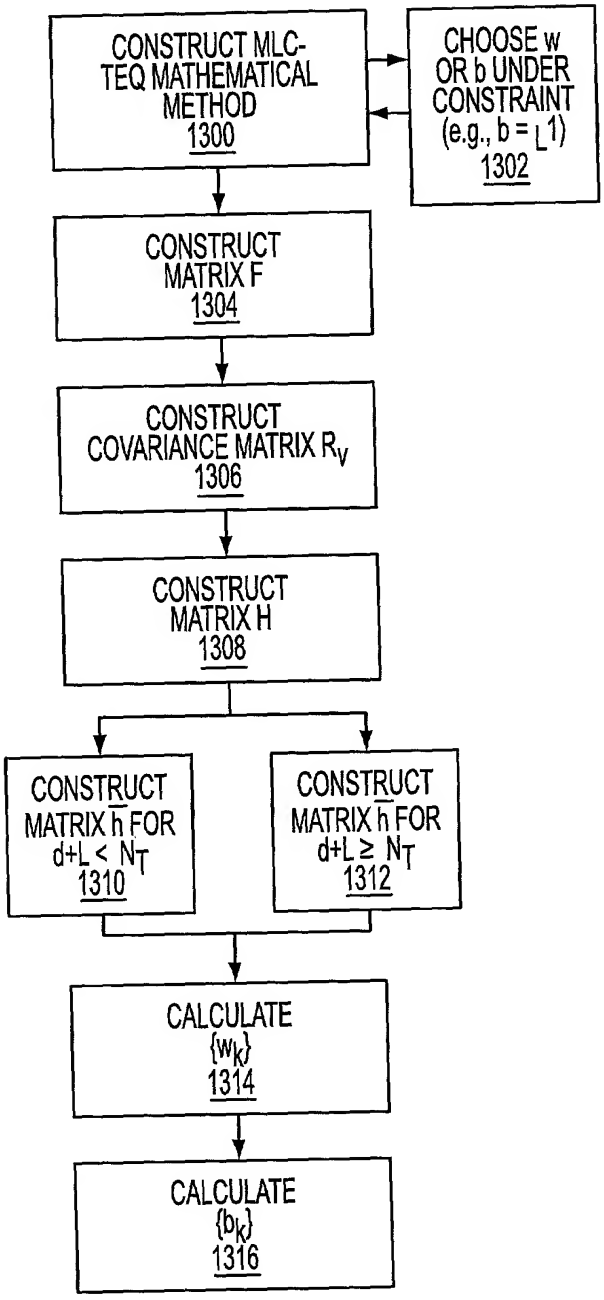
CONSTRUCT MLC-TEQ MATHEMATICAL METHOD 1300
CHOOSE w OR b UNDER CONSTRAINT (e.g., b = L1) 1302
CONSTRUCT MATRIX F 1304
CONSTRUCT COVARIANCE MATRIX R_V 1306
CONSTRUCT MATRIX H 1308
CONSTRUCT MATRIX $\bar{h}$ FOR $d+L < N_T$ 1310
CONSTRUCT MATRIX $\bar{h}$ FOR $d+L \geq N_T$ 1312
CALCULATE $\{w_k\}$ 1314
CALCULATE $\{b_k\}$ 1316

FIG. 13

20020927

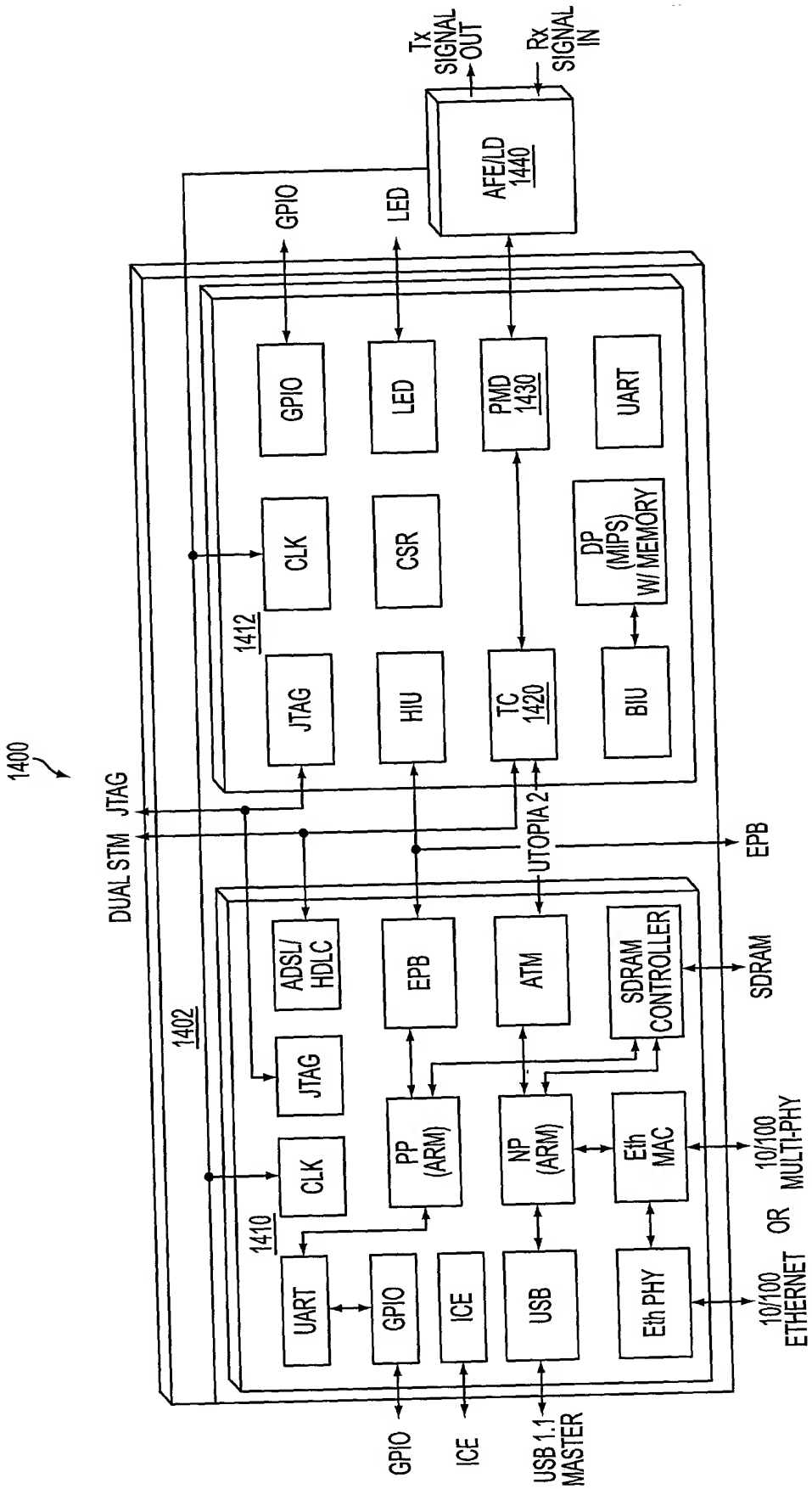

FIG. 14A

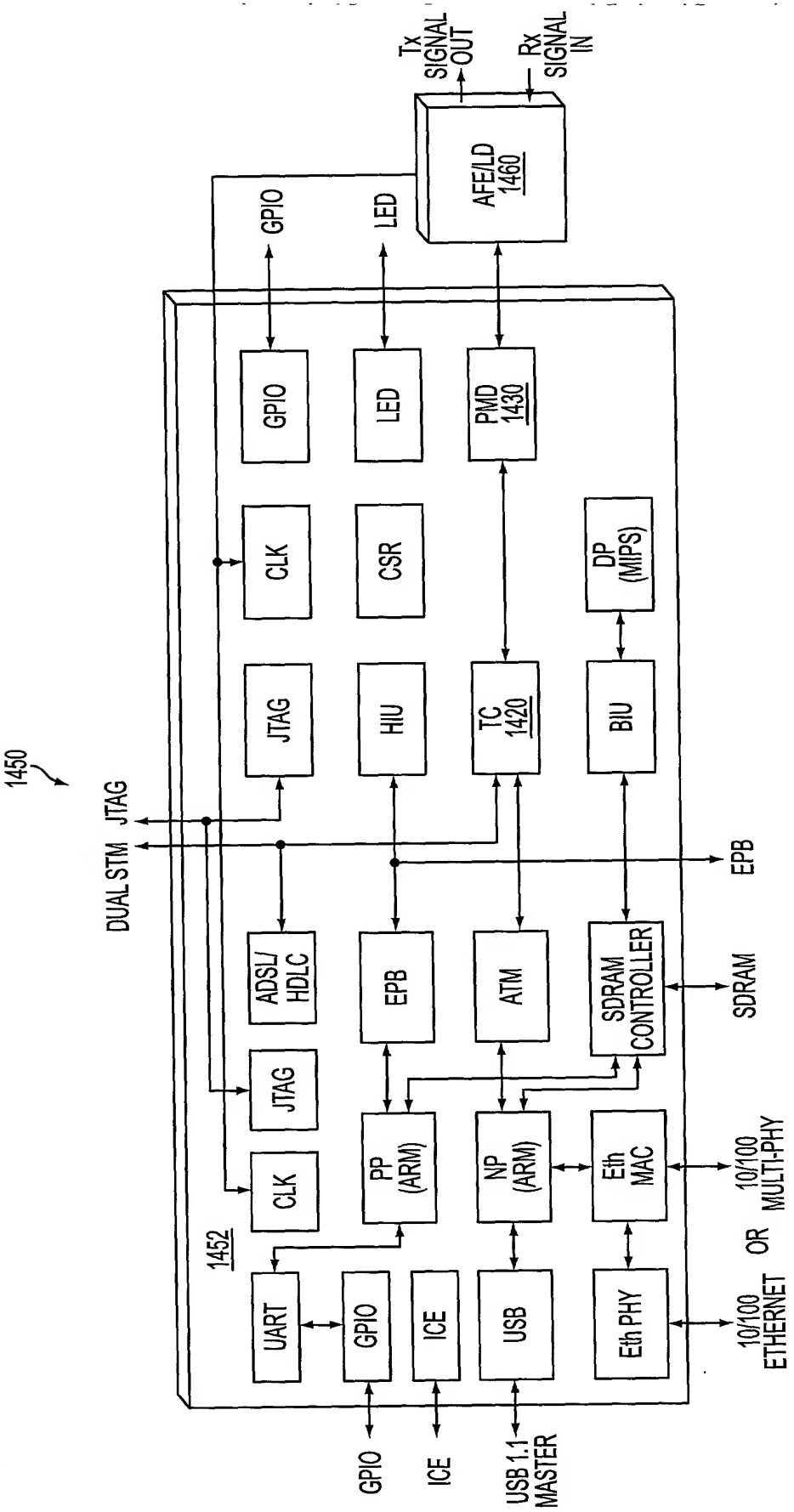
1450
DUAL STM JTAG
Tx SIGNAL OUT
Rx SIGNAL IN
AFE/LD 1460
GPIO
LED
PMD 1430
CLK
CSR
DP (MIPS)
JTAG
HIU
TC 1420
BIU
EPB
ADSL/ HDLC
EPB
ATM
SDRAM CONTROLLER
SDRAM
JTAG
CLK
PP (ARM)
NP (ARM)
Eth MAC
10/100 MULTI-PHY
OR
1452
UART
GPIO
ICE
USB
Eth PHY
10/100 ETHERNET
GPIO
ICE
USB 1.1 MASTER

FIG. 14B

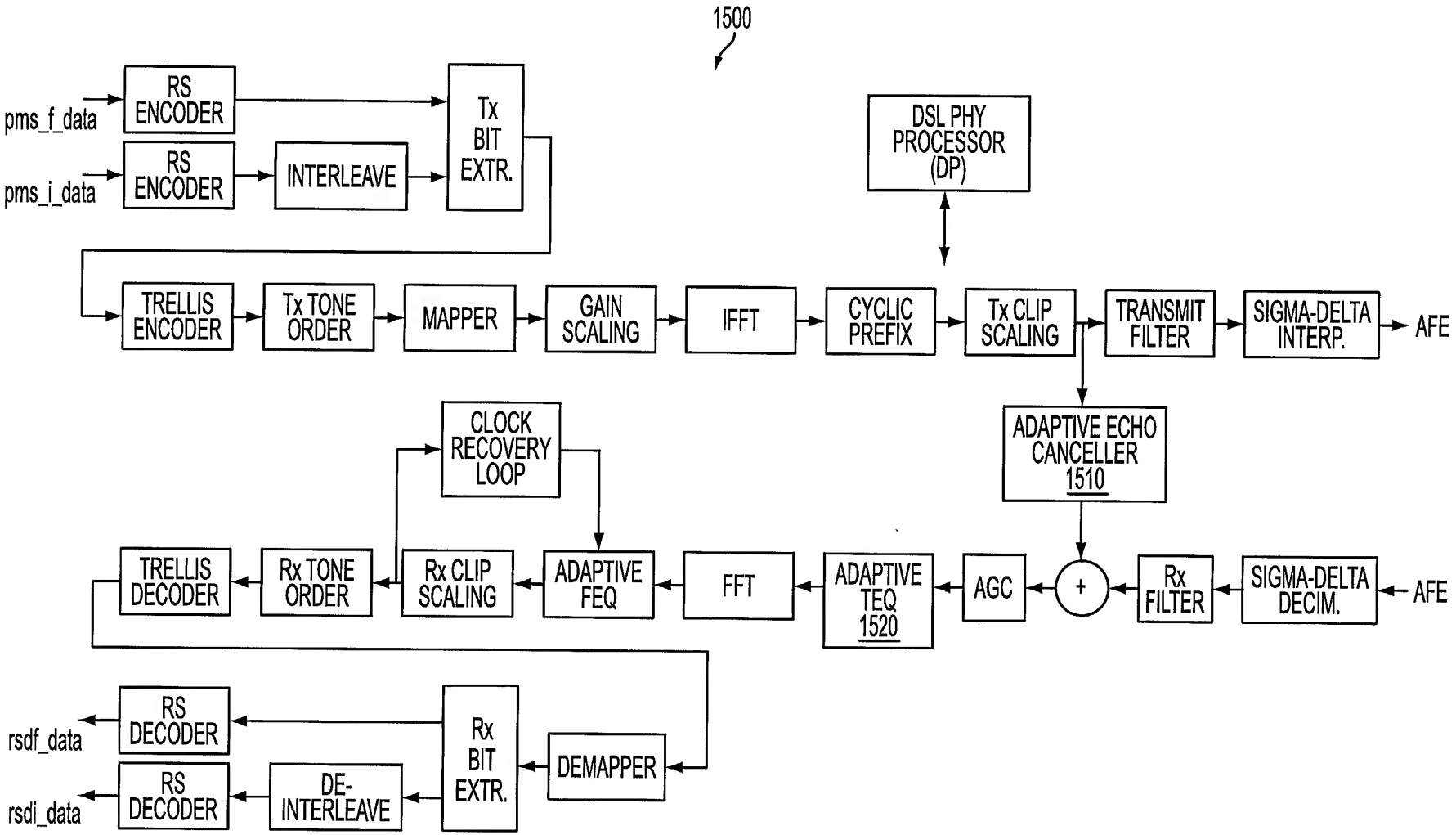
1500
pms_f_data
RS ENCODER
pms_i_data
RS ENCODER
INTERLEAVE
Tx BIT EXTR.
DSL PHY PROCESSOR (DP)
TRELLIS ENCODER
Tx TONE ORDER
MAPPER
GAIN SCALING
IFFT
CYCLIC PREFIX
Tx CLIP SCALING
TRANSMIT FILTER
SIGMA-DELTA INTERP.
AFE
CLOCK RECOVERY LOOP
ADAPTIVE ECHO CANCELLER 1510
TRELLIS DECODER
Rx TONE ORDER
Rx CLIP SCALING
ADAPTIVE FEQ
FFT
ADAPTIVE TEQ 1520
AGC
+
Rx FILTER
SIGMA-DELTA DECIM.
AFE
rsdf_data
RS DECODER
rsdi_data
RS DECODER
DE-INTERLEAVE
Rx BIT EXTR.
DEMAPPER

FIG. 15

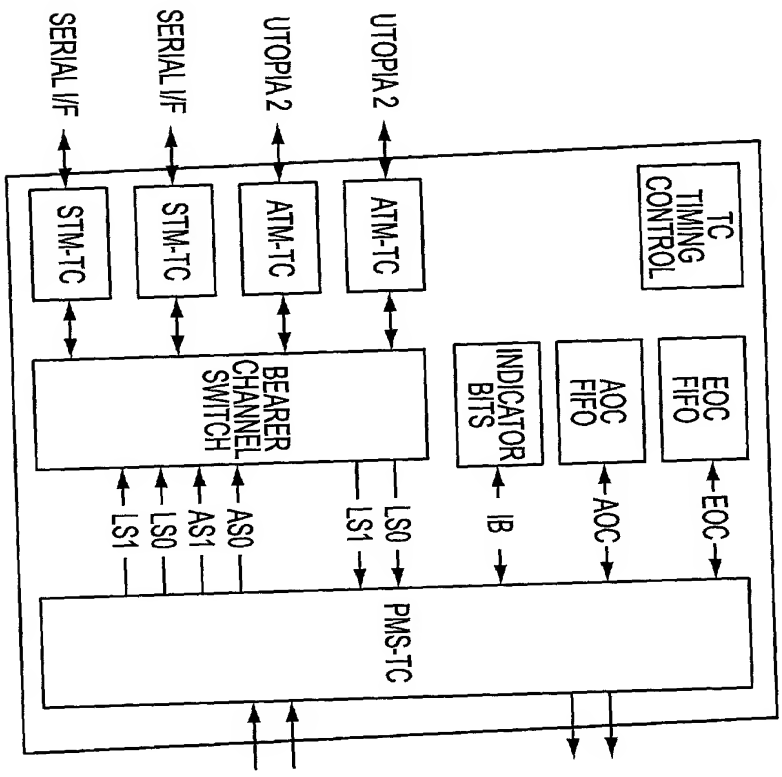

FIG. 16

Appx432-03259

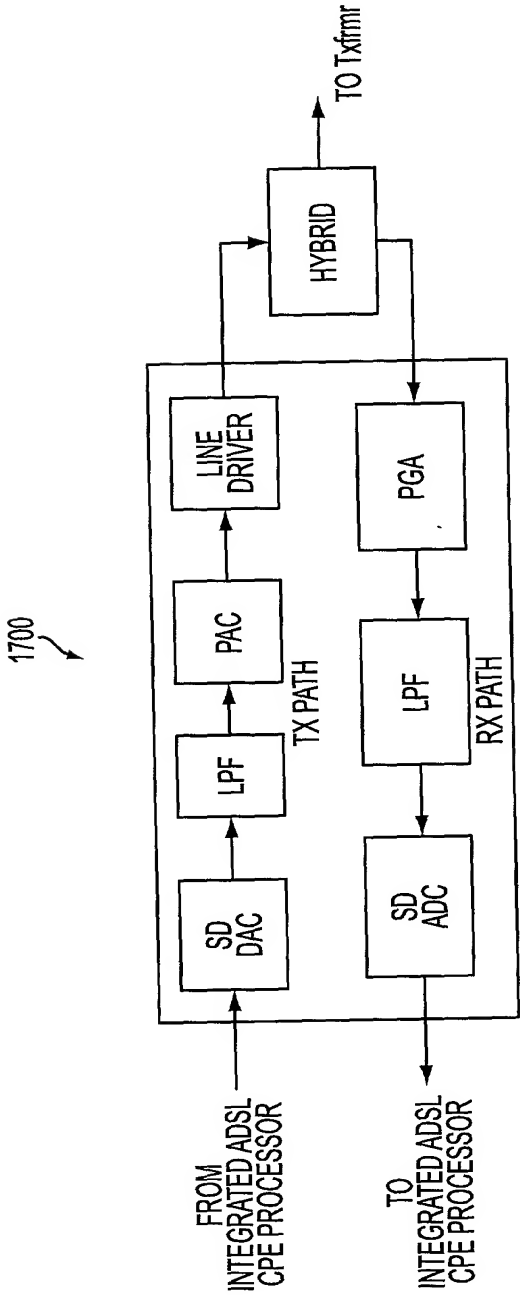
1700
TO Txfmr
HYBRID
LINE DRIVER
PAC
LPF
SD DAC
TX PATH
PGA
LPF
SD ADC
RX PATH
FROM INTEGRATED ADSL CPE PROCESSOR
TO INTEGRATED ADSL CPE PROCESSOR

FIG. 17

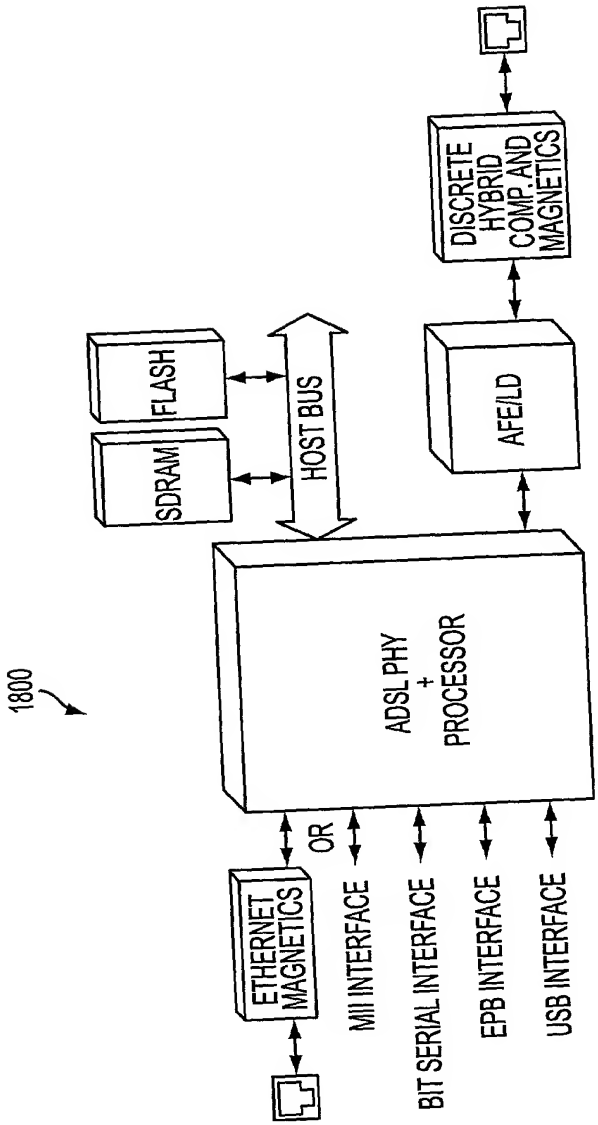
1800
ADSL PHY + PROCESSOR
FLASH
SDRAM
HOST BUS
AFE/LD
DISCRETE HYBRID COMP. AND MAGNETICS
ETHERNET MAGNETICS
OR
MII INTERFACE
BIT SERIAL INTERFACE
EPB INTERFACE
USB INTERFACE

FIG. 18A

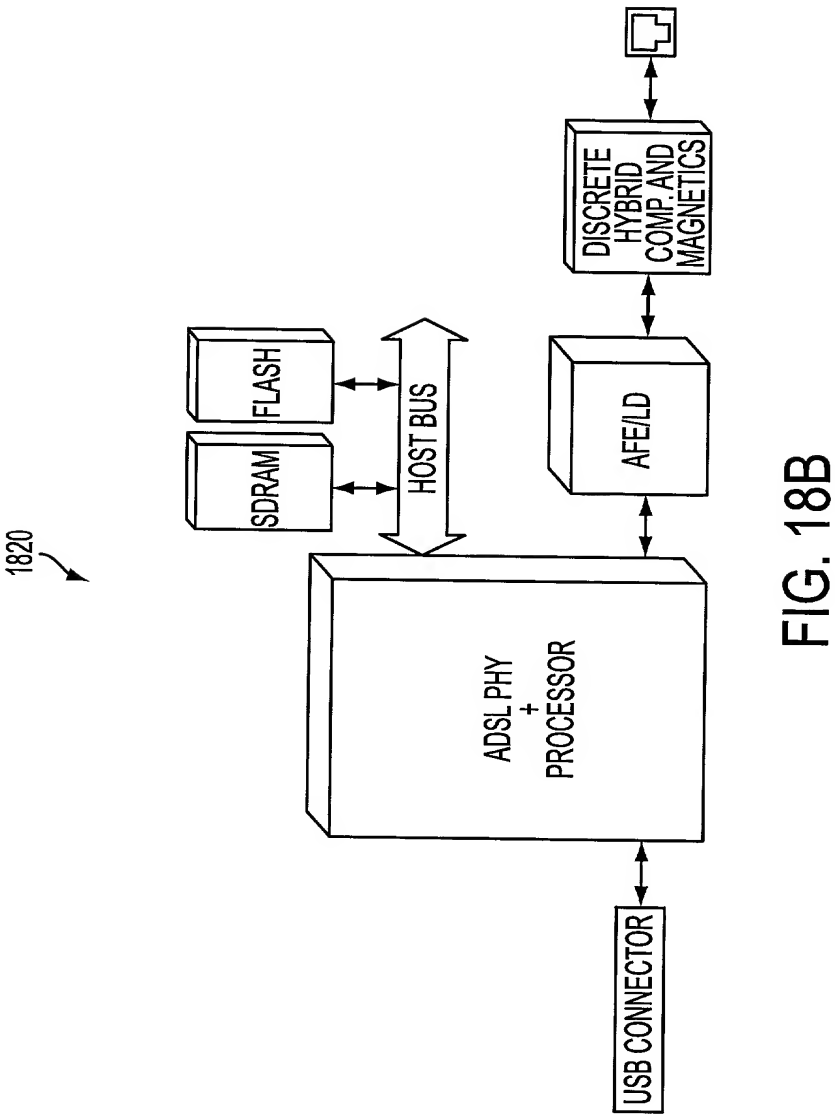
1820
FLASH
SDRAM
HOST BUS
DISCRETE HYBRID COMP. AND MAGNETICS
AFE/LD
ADSL PHY + PROCESSOR
USB CONNECTOR

FIG. 18B

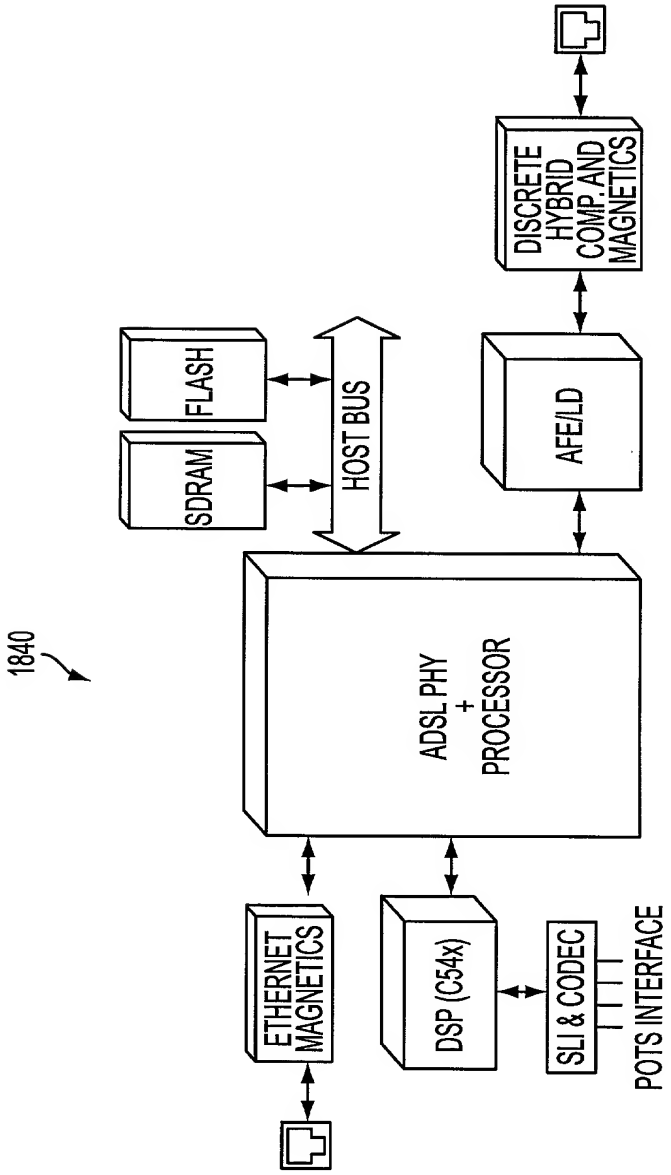
1840
ADSL PHY
+
PROCESSOR
ETHERNET MAGNETICS
DSP (C54x)
SLI & CODEC
POTS INTERFACE
FLASH
SDRAM
HOST BUS
AFE/LD
DISCRETE HYBRID COMP. AND MAGNETICS

FIG. 18C